MASK EDA WORKSHOP

11-12 July 2001
San Francisco

INTERNATIONAL SEMATECH

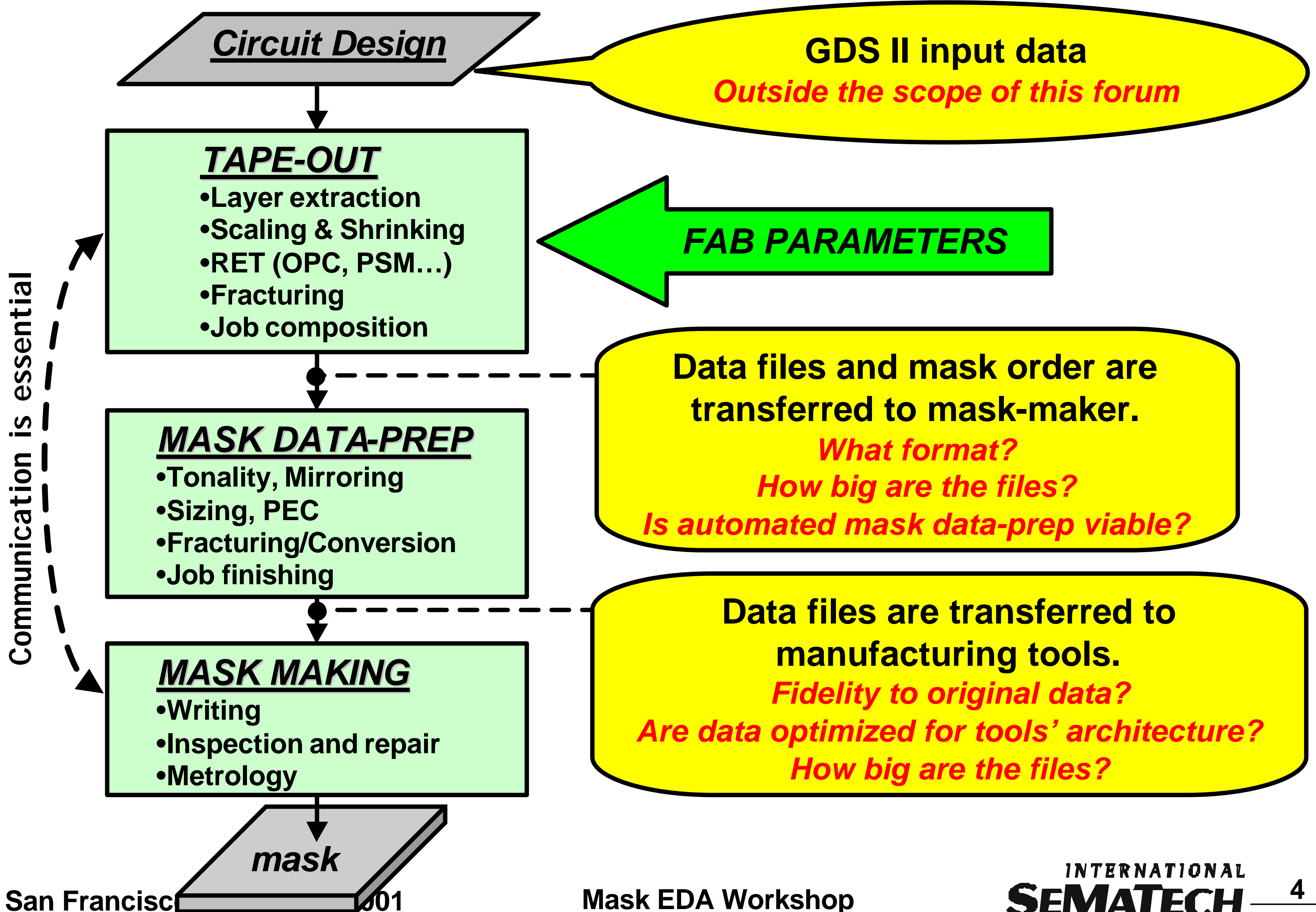
Flag Raised by ISMT Members in 9/00
MASC meeting

- **Good initial discussion on several issues**
  - Data volume is escalating too rapidly (e.g. 50 GByte)
    - Driven by the extensive use of aggressive OPC strategies
    - Data are flattened too early in the process flow
  - Proliferation of data-formats leads to inefficient data process flows
    - Lack of flexibility
    - Cumbersome order entry and error-prone conversions
  - Data related issues are a common and general problem
    - Tape-out and mask-makers
- **More homework and investigation was needed**
  - Involve the experts
  - Promote wider, global participation

1/17/01 MASC, Data-Prep Session

- **Open, cooperative discussion on mask data preparation**
- **Educated discussion among experts**
  - More than 60 people attended, mostly data-prep experts
- **Unbiased discussion among users**
  - It was homework time to define and prioritize issues
  - Not ready to involve EDA and equipment vendors
- **Issues were evaluated from different perspectives**
  - IC companies with and without captive mask-shop
  - Commercial mask-makers
  - Different chip technologies (MPU, memory, ASIC, SoC…)
  - Diverse mask-making tools for write, inspect, metrology…

Schematic Data Process Flow



1/17/01 MASC, Data-Prep Session
Issues

Escalating data volume

- **Effects:**
  - Increased tape-out turn around time
  - Increased data transfer time
  - Increased capital spending due to h/w and s/w limitations
  - Increased mask manufacturing turn around time
- **Drivers:**
  - Aggressive OPC strategies
  - Hierarchy is destroyed too early in the data process flow
- **Potential improvements and solutions:**
  - Focus on effective & manufacturable OPC strategies
    - Multidisciplinary effort
    - Include manufacturing rules at the OPC application stage
  - Full hierarchy in OPC application processes (i.e. better file size efficiency)
  - Maintain hierarchy up to the manufacturing tool

1/17/01 MASC, Data-Prep Session

Issues

Old computing architectures

- **Effects:**
  - Long tape-out and mask data-prep turn around time
  - Limited flexibility
  - Early obsolescence $\Rightarrow$ increased capital spending
- **Drivers:**
  - Legacy and history
  - Not clear consensus on alternatives among the users
- **Potential improvements and solutions:**
  - Scalable, parallel processing on spatially partitioned design
  - Software for 64-bit architectures

1/17/01 MASC, Data-Prep Session

Issues

Lack of a standard hierarchical data format

- **Effects:**
  - Mask makers have less flexibility in tools' utilization
  - Errors and anomalies may be generated during final conversion
  - Data not optimized for the designated writing architecture
  - Larger data volume to be handled
  - Order entry is cumbersome and differentiated by customer
- **Drivers:**
  - Data is flattened too early in the process flow
  - New data formats introduced with new generation write-tools
  - Lack of consensus on standardization process and objective
- **Potential improvements and solutions:**
  - Create a standard based on GDS II or on new hierarchical, compact format
    - Mask-making tools to accept input data in the new standard
  - Provide mask-maker with ready-to-write data

1/17/01 MASC, Data-Prep Session
Issues

Data conversion and data integrity

- **Effects:**
  - Feature distortion due to grid snapping
  - Is conversion fully optimized for diverse writing architectures?
- **Drivers:**
  - Aggressive OPC's driving toward gridless designs
  - Angled lines (i.e. odd angles) are common in critical features
  - New data formats introduced with new generation mask-making tools
- **Potential improvements and solutions:**
  - Gridless processing capability
  - Reliable fracturing into *Variable Shaped Beam* formats
  - Hierarchical standard (e.g. GDS II) as input format for mask-making tools

Mask EDA Workshop
Purpose

- Forum where users, vendors, and equipment makers can discuss and confront perspectives and ideas on mask EDA topics.
- Improve mutual understanding among the players, and decrease misconceptions
- Have a snapshot of the existing data related initiatives pursued around the world

Mask EDA Workshop
Expected Outcome

- **Driving factors in mask EDA issues**
- **Clear needs and requirements**
- **Viable improvement and solution paths**
- **Limits and constraints**
  - What can reasonably be required or expected
- **Increased awareness on global initiatives in mask data topics.**

Mask EDA Workshop
Attendance

EDA users
- Agere Systems
- Dai Nippon Printing
- DuPont Photomasks
- Infineon Technologies
- Intel Corporation
- Motorola
- STMicroelectronics
- Texas Instruments
- Toppan Electronics
- TSMC

EDA vendors
- ASML MaskTools
- Avant!
- Cadence Design Systems
- K2 Technologies
- Mentor Graphics
- Numerical Technologies
- Transcription Enterprises

Equipment makers
- Etec Systems
- Leica Microsystems Litho
- Micronic
- Toshiba

Others
- Int. Sematech
- SELETE
- SEMI
- SI2

Workshop Structure

- **General session**
  - Open to all attendees
- **Breakout sessions**
  - All are invited to participate by expressing their opinions and ideas
  - Summaries will be presented at the beginning of Day 2
- **EDA vendors' private sessions**
  - Each vendor will have a dedicated room
  - Opportunity for technical clarifications and follow-ups
  - Opportunity for sharing more information
  - Opportunity for collecting tailored feedback
- **Conclusive discussion**
  - Open to all attendees
  - Opportunity for final feedback and remarks
- **International SEMATECH closed session**
  - Working lunch for ISMT member companies only

Mask EDA Workshop

Agenda, Day 1

Wednesday, 11 July 2001				
GENERAL SESSION	7:00 - 8:00	am	Breakfast	
	8:00 - 8:30	am	Introduction and Summary of 1/17/01 mask data mtg	G. Bianucci
	8:30 - 8:45	am	DuPont Photomasks	P. Buck
	8:45 - 9:00	am	Intel	B. Gleason
	9:00 - 9:15	am	Motorola	A. Reich
	9:15 - 9:45	am	Infineon: Automops - introduction and demo	G. Ballhorn
	9:45 - 10:15	am	Break	
	10:15 - 10:45	am	Avant!	M. Rieger
	10:45 - 11:15	am	Cadence	B. Pack
	11:15 - 11:45	am	K2 Technologies	D. Rogers
	11:45 - 12:15	am	MaskTools	K. Wampler
	12:15 - 1:30	pm	Lunch	*Monterey*
	1:30 - 2:00	pm	Mentor Graphics	L. Anderson
	2:00 - 2:30	pm	Numerical Technologies	L. Karklin
	2:30 - 3:00	pm	Transcription Enterprises	K. MacLean
	3:00 - 3:15	pm	Break	
BREAK OUT SESSIONS	3:15 - 4:45	pm	File size efficiency in OPC application tools	*Presidio*
	3:15 - 4:45	pm	Alternative computing technologies and architectures	*Sutter*
	3:15 - 4:45	pm	Data format standardization	*Grant*
	4:45	pm	Breakout and general sessions adjourn	
VENDORS' PRIVATE SESSIONS	5:00 - 6:30	pm	Avant!	*Monterey*
	5:00 - 6:30	pm	Cadence	*Grant*
	5:00 - 6:30	pm	K2 Technologies	*Sacramento*
	5:00 - 6:30	pm	MaskTools	*Sutter*
	5:00 - 6:30	pm	Mentor Graphics	*Sonoma*
	5:00 - 6:30	pm	Numerical Technologies & Transcription Enterprises	*Montgomery*
	6:30	pm	Dinner	*California Parlor*

Mask EDA Workshop

Agenda, Day 2

	Thursday, 12 July 2001			
GENERAL SESSION	7:00 - 8:00	am	Breakfast	
	8:00 - 9:00	am	Summary of breakout sessions	Facilitators
	9:00 - 9:15	am	Leica	O. Fortagne
	9:15 - 9:30	am	Etec	
	9:30 - 9:45	am	Micronic	J. Freyer
	9:45 - 10:00	am	Toshiba	T. Takigawa
	10:00 - 10:25	am	Break	
	10:25 - 10:45	am	Mask data initiatives at SELETE	K. Kuriyama
	10:45 - 11:00	am	SEMI task force on data-path constraints	T. Grebinski
	11:00 - 12:15	pm	Conclusive discussion and closure remarks	All
	12:15	pm	Adjourn	
	12:15 - 2:00	pm	Working lunch for ISMT members only	*Presidio*

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